

Message Text

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ORIGIN COME-00

INFO OCT-01 CIAE-00 DODE-00 EB-11 NSAE-00 RSC-01 TRSE-00

EUR-25 AEC-11 ISO-00 MC-02 /051 R

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APPROVED BY EB/ITP/EWT:JMGREGORY,JR.

COMMERCE/OEA:CSEASWORD

RPE

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R 021702Z MAY 74

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C O N F I D E N T I A L STATE 090210

EXCON

E.O. 11652: XGDS-1

TAGS: ESTC, COCOM, US, UR

SUBJECT: US COMPUTER SYSTEM TO USSR - IL 1565

REF: A) COCOM DOC (74)535

B) COCOM DOC (74)679

C) STATE 81649

D) COCOM DOC (74)806 REVISED

IN A PREVIOUS COMMUNICATION (REF C) US TECHNICIANS CONFIRMED THAT THE MAIN MEMORY MODULES IN THE SUBJECT B6700 COMPUTER SYSTEM WERE NOT INTERLEAVED. THE FOLLOWING IS AN EXPLANATORY STATEMENT OF WHY THIS IS SO:

INTERLEAVING OF MAIN MEMORY MODULES OF THE B6700 IS ACCOMPLISHED BY EXCHANGING THE LOW ORDER BIT OF THE MODULE ADDRESS WITH THE LOW ORDER BIT OF THE WORD ADDRESS. THIS IS DONE BY LOCAL CABLE EXCHANGE BETWEEN ADJACENT MEMORY MODULES WHICH MUST BE OF THE SAME SPEED, WORD SIZE AND MODULE SIZE. INTERLEAVING OF 1.2 MICROSECOND AND 1.6 MICROSECOND MEMORIES IS INEFFECTUAL.

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THE B6700 SYSTEM PROPOSED FOR EXPORT INCLUDES TWO 1-2 MICRO-

SECOND MEMORIES AND ONE 1.6 MICROSECOND MEMORY. THE MASTER CONTROL PROGRAM PLACES THE "SAVE OBJECT CODE" IN LOW MEMORY AND THE "SAVE MEMORY TABLES" IN HIGH MEMORY. SINCE THESE LOW AND HIGH MEMORY AREAS ARE THE OBJECT OF THIRTY PERCENT OF ALL SYSTEM MEMORY ACCESSES, THIS B6700 SYSTEM HAS BEEN CONFIGURED WITH THE TWO 1.2 MICROSECOND MEMORY MODULES IN THE HIGH AND LOW ADDRESS POSITIONS SEPARATED IN THE MIDDLE BY THE 1.6 MICROSECOND MEMORY. ACTUAL PERFORMANCE TESTS AND USAGE EXPERIENCE INDICATE THAT ONLY A SMALL IMPROVEMENT COULD BE OBTAINED FROM INTERLEAVED OPERATION ON A B67 SYSTEM OF THE TYPE PROPOSED FOR EXPORT. THE PRIMARY REASON FOR THE SMALL GAIN IS THE INABILITY OF THE CPU TO MAKE TWO SUCCESSIVE MEMORY ACCESSIONS IN ONE MEMORY CYCLE. AN AVERAGE OF THREE INSTRUCTIONS ARE STORED IN A SINGLE MEMORY WORD EACH OF WHICH REQUIRED TWO OR MORE CLOCK CYCLES FOR EXECUTION. FOR THIS AND OTHER REASONS IT IS RARE THAT REQUESTS FOR TWO SUCCESSIVE MEMORY WORDS CAN BE MADE BY THE CPU. BECAUSE OF (1) THE MEMORY SPACE ALLOCATION MADE BY THE MASTER CONTROL PROGRAM AND (2) THE SMALL INCREASE IN PERFORMANCE THAT WOULD RESULT IF MEMORY WERE INTERLEAVED, THE EXPORTER HAS MADE A BASIC DECISION TO CONFIGURE THIS SYSTEM IN SUCH A WAY THAT INTERLEAVING CANNOT BE IMPLEMENTED. RUSH

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Message Attributes

Automatic Decaptioning: X
Capture Date: 01 JAN 1994
Channel Indicators: n/a
Current Classification: UNCLASSIFIED
Concepts: DATA PROCESSING EQUIPMENT, STRATEGIC TRADE CONTROLS, COMPUTERS
Control Number: n/a
Copy: SINGLE
Draft Date: 02 MAY 1974
Decaption Date: 01 JAN 1960
Decaption Note:
Disposition Action: RELEASED
Disposition Approved on Date:
Disposition Authority: garlanwa
Disposition Case Number: n/a
Disposition Comment: 25 YEAR REVIEW
Disposition Date: 28 MAY 2004
Disposition Event:
Disposition History: n/a
Disposition Reason:
Disposition Remarks:
Document Number: 1974STATE090210
Document Source: CORE
Document Unique ID: 00
Drafter: MKRAVETZ:CLK
Enclosure: n/a
Executive Order: X1
Errors: N/A
Film Number: D740106-0148
From: STATE
Handling Restrictions: n/a
Image Path:
ISecure: 1
Legacy Key: link1974/newtext/t19740579/aaaacsxa.tel
Line Count: 85
Locator: TEXT ON-LINE, ON MICROFILM
Office: ORIGIN COME
Original Classification: CONFIDENTIAL
Original Handling Restrictions: n/a
Original Previous Classification: n/a
Original Previous Handling Restrictions: n/a
Page Count: 2
Previous Channel Indicators:
Previous Classification: CONFIDENTIAL
Previous Handling Restrictions: n/a
Reference: A) COCOM DOC (74)535
Review Action: RELEASED, APPROVED
Review Authority: garlanwa
Review Comment: n/a
Review Content Flags:
Review Date: 19 APR 2002
Review Event:
Review Exemptions: n/a
Review History: RELEASED <19 APR 2002 by shawdg>; APPROVED <17 JAN 2003 by garlanwa>
Review Markings:

Declassified/Released
US Department of State
EO Systematic Review
30 JUN 2005

Review Media Identifier:
Review Referrals: n/a
Review Release Date: n/a
Review Release Event: n/a
Review Transfer Date:
Review Withdrawn Fields: n/a
Secure: OPEN
Status: NATIVE
Subject: US COMPUTER SYSTEM TO USSR - IL 1565
TAGS: ESTC, US, UR, COCOM
To: OECD PARIS
Type: TE
Markings: Declassified/Released US Department of State EO Systematic Review 30 JUN 2005